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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/385,959	08/30/1999	TOSHIHARU YANAGIDA	P99.1318	9858

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

CA

Office Action Summary	Application No.	Applicant(s)	
	09/385,959	YANAGIDA, TOSHIHARU	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-21* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

In the rejections infra, reference labels are generally recited only for the first recitation of identical elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 10, 11, 16 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hayes (6114187), Hotchkiss (2002/0106832) and Behun (5147084).

At column 5, line 23 to column 7, line 48, and column 9, lines 1-35, Hayes teaches the following limitations of independent claim 7:

A method of producing of a semiconductor apparatus, the method comprising the steps of: forming metal bumps 3 in direct contact with a circuit pattern of a semiconductor device 1 formed on a semiconductor substrate 17 in a wafer state; forming a resin film 4 on a circuit pattern forming surface of said semiconductor device so as to seal spaces between said metal bumps and to become thinner than a height of the metal bumps; cleaning the surfaces of the metal bumps projecting out from the resin film; after the cleaning step, forming eutectic solder layers 9 different in composition from the metal bumps on the surfaces of the metal bumps;

after the forming solder layers step, cutting the semiconductor wafer into unit semiconductor chips 1, each semiconductor chip having at least one of said semiconductor device; and after the cutting step, mounting at least one of the semiconductor chips on a mounting "substrate" (not labeled) from a bump forming surface side of the semiconductor chip so as to connect the eutectic solder layers of the semiconductor chip to the mounting substrate "flip-chip fabrication."

However, Hayes does not appear to explicitly teach forming metal ball bumps in direct contact with the circuit pattern.

Still, Hayes teaches forming metal columns 3 in direct contact with the circuit pattern. In addition, at paragraphs 33-36, Hotchkiss teaches attaching metal ball bumps 114 directly to an integrated circuit. Furthermore, it would have been obvious to substitute the metal ball bumps of Hotchkiss for the metal columns of Hayes because Hotchkiss teaches that metal columns and metal ball bumps are equivalents used for the same purpose of electrical connection in a flip-chip process.

Also, although Hayes teaches mounting at least one of the semiconductor chips on a mounting substrate, Hayes does not appear to explicitly teach a mounting board substrate.

Nonetheless, as cited supra, Hotchkiss teaches mounting a semiconductor chip 112 on a mounting "board" (not labeled) substrate. In

addition, it would have been obvious to combine the process of Hotchkiss with the process of Hayes because it would provide a mounting substrate.

Hayes also does not appear to explicitly teach mounting the semiconductor chip on the mounting board with the resin film directly contacting the semiconductor chip and not directly contacting the mounting board.

Notwithstanding, at column 3, lines 38-62, column 5, lines 7-12, and column 5, line 41 to column 6, line 15, Behun teaches mounting a semiconductor chip 10 on a mounting board 11 with the resin film 20 directly contacting the semiconductor chip and not directly contacting the mounting board. Furthermore, it would have been obvious to combine the processes of Behun with the applied prior art because, as taught by Behun, it would facilitate reworkability and heat dissipation.

As cited, Hayes also teaches a process of production of a semiconductor apparatus wherein, in said cleaning step, the surfaces are cleaned by removing components inviting a rise in a connection resistance and a decline in a joint strength at least at a connection interface; in said cleaning step, any resin film components deposited on said bumps are removed; in said cleaning step, oxides on said bump surfaces are removed; in said cleaning step, the cleaning of the surfaces of the bumps is performed by irradiating a laser beam; the metal ball bumps formed in the first step are

solder bumps; said solder bumps have a melting point higher than a melting point of said eutectic solder and said eutectic solder layers are comprised of a eutectic solder; and in said forming solder layers step, the eutectic solder layers are formed by a printing method, plating method, or transfer method.

To further clarify the teachings wherein the surfaces are cleaned by removing components inviting a rise in a connection resistance and a decline in a joint strength at least at a connection interface, and oxides on said bump surfaces are removed, it is noted that these processes are inherent results of the cleaning process of Hayes.

Claims 12, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hayes, Hotchkiss and Behun as applied to claims 7, 8, 10, 11, 16 and 19-21, and further in combination with Nishikawa (6227436) and Denning (6187682).

The combination of Hayes, Hotchkiss and Behun does not appear to explicitly teach a process of production of a semiconductor apparatus wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed by plasma cleaning; said plasma cleaning is at least sputter etching by discharge plasma of an inert gas; and the cleaning of the surfaces of the bumps is performed under a reduced pressure atmosphere, an inert gas atmosphere, or a reducing gas atmosphere.

Nevertheless, at column 5, line 62 to column 6, line 67, Nishikawa teaches a process of production of a semiconductor apparatus 1 wherein cleaning of the surfaces of bumps 9 is performed by sputter etching of an inert gas ("argon"). Moreover, it would have been obvious to combine the process of Nishikawa with the process of the applied prior art because it would enable cleaning of the surfaces of the bumps 3.

However, the combination of Hayes, Hotchkiss, Behun and Nishikawa does not appear to explicitly teach that the sputter etching is by discharge plasma.

Regardless, at column 2, line 66 to column 5, line 50, Denning teaches a process of sputter etching by discharge plasma. Furthermore, it would have been obvious to combine the process of Denning with the process of the applied prior art because it would enable sputter etching.

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hayes, Hotchkiss, Nishikawa, Behun and Denning as applied to claims 12, 13 and 17, and further in combination with Okumura (4807021).

The prior art applied to claims 12, 13 and 17 does not appear to explicitly teach a process of production of a semiconductor wherein said plasma cleaning is at least oxygen plasma treatment and then sputter etching by discharge plasma of an inert gas; and wherein said plasma

cleaning is at least oxygen plasma treatment and then sputter etching by discharge plasma of a reducing gas.

However, as cited supra, Denning teaches a process wherein plasma cleaning is sputter etching by discharge plasma of an inert and a reducing gas. Moreover, it would have been obvious to combine the process of Denning with the process of the applied prior art because it would enable cleaning.

Also, at column 5, lines 32-44, Okumura teaches a process of production of a semiconductor apparatus wherein plasma cleaning is at least oxygen plasma treatment. In addition, it would have been obvious to combine the process of Okumura with the process of the applied prior art because it would enable cleaning.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayes, Hotchkiss and Behun as applied to claims 7, 8, 10, 11, 16 and 19-21, and further in combination with Jackson (5068040).

The combination of Hayes, Hotchkiss and Behun does not appear to explicitly teach wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed while applying a gas jet to the bumps to peel off the unnecessary components which are then sucked away.

Notwithstanding, at column 4, line 44 to column 5, line 33; and column 7, line 46 to column 8, lines 49, Jackson teaches a process wherein

the cleaning of the surfaces of a semiconductor apparatus is performed while applying a gas jet to the apparatus to peel off the unnecessary components which are then sucked 28 away. Additionally, it would have been obvious to combine the process of Jackson with the process of the applied prior art because it would enable cleaning.

Applicant's remarks filed 5-24-4 have been fully considered and are addressed in the rejection supra and further addressed infra.

Applicant alleges that the rejection, "argues that since *Hotchkiss* discloses metal ball bumps 114 formed in direct contact with a circuit pattern, metal ball bumps are allegedly substitutes for solder columns, and therefore, it allegedly would have been obvious to substitute *Hayes's* solder columns with metal ball bumps to allegedly disclose or suggest Applicant's claimed metal ball bumps having eutectic solder layers formed thereon."

This allegation is respectfully traversed because Hotchkiss is not relied on in the rejection for the rejection for a disclosure of metal ball bumps having eutectic solder layers formed thereon, and the rejection does not present this alleged argument. Instead, the rejection argues that, "it would have been obvious to substitute the metal ball bumps of Hotchkiss for the metal columns of Hayes because Hotchkiss teaches that metal columns and metal ball bumps are equivalents used for the same purpose of electrical connection in a flip-chip process."

Relatedly, applicant contends that the columns of Hayes and the bumps of Hotchkiss "do not serve the same purpose."

This contention is respectfully traversed because, as explicitly and clearly set forth in the rejection, "Hotchkiss teaches that metal columns and metal ball bumps are equivalents used for the same purpose of electrical connection in a flip-chip process."

In addition, appellant proffers particular advantages for the instant claimed invention.

Regardless, it is respectfully submitted that reasons for, or advantages resulting from, doing what the applied prior art has suggested, is not demonstrative of nonobviousness. In re Kronig 190 USPQ 425, 428 (CCPA 1976); In re Lintner 173 USPQ 560 (CCPA 1972). Indeed, the prior art teaches the claimed invention; therefore, the alleged reason or advantage is an inherent result of the prior art process. Furthermore, the prior art motivation or advantage may be different than that of applicant while still supporting a conclusion of obviousness. In re Wiseman 201 USPQ 658 (CCPA 1979); Ex Parte Obiaya 227 USPQ 58 (Bd. of App. 1985).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a

first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Head SAE Linda Hodge-Taylor whose telephone number is 571-272-1585.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
8-Aug-04